Kadi Sarva Vishwavidyalaya

Faculty of Engineering & Technology

Second Year Bachelor of Engineering (CE/IT) – Semester III

(With effect from: Academic Year 2018-19)

Subject Code: CT304-N	**Subject Title:** Digital Electronics
Pre-requisite	

Teaching Scheme (Credits and Hours)

Teaching Scheme				Total Credit	Evaluation Scheme					
L	T	P	Total		Theory		Mid Sem Exam	CIA	Practical	Total
Hours	Hours	Hours	Hours		Hours	Marks	Marks	Marks	Marks	Marks
04	00	02	06	05	03	70	30	20	30	150

Learning Objectives:

- Develop understanding of number systems and Boolean algebra.
- Understand the functioning of logic gates, their implementation and verification of truth tables.
- Develop the understanding of the working of different combinational logic circuits.
- Understand and verify the working of various sequential logic circuits.
- Understand simulation tools for digital logic circuits and simulation of digital logic circuits.
- Understand and design circuit using finite state machine.
- Understand and verify the working of Various Types of D/A and A/D converters

Outline of the Course:

Sr. No	Title of the Unit	Minimum Hours
1	Number Systems and Codes	07
2	Boolean Algebra and Logic Gates	12
3	Combinational Logic Circuit	08
4	Flip Flops and Sequential Logic and Circuits	14
5	Introduction to State Machines	12
6	Programmable Logic Devices	05
7	D/A and A/D Converters	06
	Total	**64**

Total hours (Theory): 64
Total hours (Lab): 32
Total hours: 96

Detailed Syllabus:

Sr. No	Topic	Lecture Hours	Weightage (%)
1	**Number Systems and Codes:** Decimal, Binary, octal, and hexa-decimal number systems, binary arithmetic. Number base conversion, Complements, Codes: Binary code, excess-3 code, gray code, error detection and correction codes.	07	12
2	**Boolean Algebra and Logic Gates:** Positive logic and Negative Logic, AND, OR, NOT, NAND, NOR, X-OR GATE, **:** Introduction, Logic Operators, Postulates and theorems, properties, Product of Sums and Sum of Products, Karnaugh Map method, Two, three, four, five variable K-maps, Converting Boolean expressions to Logic and Vice versa, NAND and NOR implementation, Don't-Care conditions, The tabulation method, Determination of Prime implicants.	12	18
3	**Combinational Logic Circuit:** Half and full Adder, Half and full Subtractor, Binary parallel adder, BCD Adder, Decimal adder, Magnitude comparator, Encoders & Decoders, Multiplexers, Demultiplexer, code conversion	08	13
4	**Flip Flops and Sequential Logic and Circuits:** Basic difference between Combinational logic and Sequential logic, Flip-Flops like S-R , J-K, D, Master Slave, Triggering of (level and Edge) flip-flops –Asynchronous and Synchronous Inputs, Excitation tables for flip-flops , Ripple and Synchronous counters, Registers, Shift registers, Pulse Generation.	14	22
5	**Introduction to State Machines:** The Need for State Machines, The State Machine, Basic Concepts in State Machine Analysis, Synchronous State Machine Design: Sequential Counters, State Changes Referenced to Clock, Number of State Flip-Flops.	12	18
6	**Programmable Logic Devices:** Introduction to Programmable Logic Devices, Read-Only Memory, Programmable Logic Arrays (PLA), Programmable Array Logic (PAL).	05	08
7	**D/A and A/D Converters:** Digital to Analog Converters D/A converter Specifications, R-2R Ladder Type DAC, binary Weighted Resistor, A/D converters, A/D Converter Specifications, A/D Converter Technology, Counter Type, Tracking Type ,Flash Type Successive Approximation and Dual slop type A/D.	06	09
	Total	64	100

Instructional Method and Pedagogy:

- At the start of course, the course delivery pattern, prerequisite of the subject will be discussed.
- Lectures will be conducted with the aid of multi-media projector, black board, OHP etc.
- Attendance is compulsory in lecture and laboratory which carries 10 marks in overall evaluation.
- One internal exam will be conducted as a part of internal theory evaluation.
- Assignments based on the course content will be given to the students for each unit and will be evaluated at regular interval evaluation.
- Surprise tests/Quizzes/Seminar/tutorial will be conducted having a share of five marks in the overall internal evaluation.
- The course includes a laboratory, where students have an opportunity to build an appreciation for the concepts being taught in lectures.
- Experiments shall be performed in the laboratory related to course contents.

Learning Outcome:

On successful completion of this course, the student should be able to:

- The student can identify different areas of Digital circuits.
- Can find the applications of all the areas in day to day life.
- Can identify the operations, working, construction, material and aspects of Digital devices, ICs, Logic Gates etc.

Reference Books:

1. M. Morris Mano- Digital logic and computer Design, PHI
2. G.K.Kharate-Digital Electronics, Oxford
3. A. Anand Kumar- Fundamentals of Digital Circuits, PHI
4. R.P.Jain- Digital Electronics, TMH
5. B. Somanathan Nair- Digital Electronics and Logic Design, PHI

List of experiments:

Sr. No.	Name of Experiment
1	To Study & verify the Truth tables of Digital logic Gates.
2	To Study And Verify Various Theorems Of Boolean Algebra Including De-Morgan's.
3	To Study and Perform the Functionality of NAND and NOR GATE AS Universal Gate.
4	To develop Adder AND SUBTRACTOR and verify its operation.
5	To verify the operation Of Decoder 1) 2 to 4 line Decoder 2) 3 to 8 line Decoder using IC-74138
6	To study and verify the Truth tables of 8:1 Multiplexer using IC 74151A.
7	To verify the operation of 4-bit comparator using ic 7485.
8	To study & perform PARITY GENRATOR / CHECKER.
9	To test the seven segments display using 7447 IC.
10	To study & Perform Different types of Flip-Flops • R-S (Reset-Set) flip-flop • Clocked R-S flip-flop • D (Delay)flip-flop • Clocked D flip-flop • J-K flip-flop • T (Toggle) flip-flop
11	To perform A/D converter
12	To perform D/A Converter.
	As part of experimentation, a small project / model / seminar / poster / other should be prepared / presented by student(s) based on the practical knowledge gained by this course at the end of the curriculum. The concerned laboratory faculty (in consultation with course coordinator) is empowered to design/decide the type/execution of this experiment. The student(s) are expected to present the same before their batch-mates.